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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,395	01/07/2002	Cheisan J. Yue	P01,0365	2072

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EXAMINER	
HU, SHOUXIANG	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,395	YUE ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20,30 and 32-40* is/are pending in the application.

4a) Of the above claim(s) *1-20 and 30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 1-20 and 30 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, according to the previous office action. As a result, claims 1-20, 30, and 32-40 are pending in this application; and claims 32-40 remain active in this Office action.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the subject matter of the capacitive switching ratio of the varactor being greater than 20 as recited in claim 40 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for

consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities and/or defects:

The instant specification state, on page 7, lines 5-7, "As can be see by the graph of Figure 4, the capacitive switching ratio of the varactor 10 in this case is on the order of 33." However, it is not consistent with what is actually shown in Fig. 4, in which the capacitive switching ratio is no larger than about 18 (36/2).

Appropriate correction is required.

Claim Objections

4. Claim 40 is objected to because of the following informalities and/or defects:

Claim 40 recites the subject matter that the capacitive switching ratio of the varactor being greater than 20, but it is not fully supported by the original disclosure, in view of the above objections to the drawings and to the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 32-40, as being best understood in view of the claim objection above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang et al. ("Chiang"; US 5,038,184) in view of Litwin et al. ("Litwin"; US 6,100,770).

Chiang discloses a method for making a varactor (see Figs. 2-3 and 7; also see col. 4, lines 26-36, col. 5, lines 14-64, and col. 7, lines 32-35), comprising: forming a plurality of alternating lightly doped wells or body (47) and heavily doped N+ region regions in a silicon layer of an SOI structure; forming a plurality of gate oxides (44); forming a plurality of polysilicon gates (46); electrically coupling each of the polysilicon gates together; and, electrically coupling each of the heavily doped second conductivity type region regions together, wherein the lightly doped wells and the heavily doped N+ regions both extend from the top to the bottom of semiconductor layer (42).

Although Chiang does not expressly disclose that the lightly doped well or body region can be P-type doped, one of ordinary skill in the art would readily recognize that the lightly doped well or body regions in an varactor can be commonly and desirably P-type lightly doped for forming a depletion-type channel region with good channel modulation sensitivity (i.e., an NMOS-enhancement-transistor-like varactor), as

evidenced in Litwin (see the P-type lightly doped well or body region (22) and the heavily doped N+ region in the varactor of Fig. 2; also see col. 4, lines 8-29).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the making of the P-type lightly doped well or body regions of Litwin into the method of Chiang, so that a method for making a varactor with a commonly desired highly sensitive depletion-type channel regions would be obtained. And, with the P-type lightly doped regions in the above collectively taught method, N+/P- junctions would be naturally formed therein.

Regarding claims 34-36, it is art-known that silicon-insulator substrates of both the silicon-on-oxide type (SOI type, which normally naturally includes a highly resistive silicon bottom layer) and the silicon-on-sapphire type (SOS) had become readily available for either N-channel or P-channel type MOS devices, as readily evidenced in the prior art such as Tsang (US 5,563,438; see col. 3, lines 36-37).

Regarding claims 38-40, Litwin further teaches that each of the silicon gates can have a width-to-length ratio in a range covering a ratio of approximately 16 to 1 (see col.6, lines 10-17), which is substantially the same ratio as that in the instant invention (as recited in claim 38), and would naturally result in a capacitor switching ratio in the collectively taught varactor substantially similar to the one of the instant invention. And, insofar as being supported by the original disclosure, it is noted that a capacitor switching ratio as high as the ones recited in the instant invention is always commonly desirable in the art and that the width-to-length ratio and the capacitor switching ratio

are both art-recognized parameters of importance subject to routine experimentation and optimization.

Response to Arguments

Applicant's arguments filed on September 27, 2004, have been fully considered but they are not persuasive.

In response to applicant's first and second arguments in the first through fourth main arguments listed in the 09-27-04 Amendment/Remarks, it is noted that Chiang expressly discloses that the ground electrode regions (45) can be "n+ type" doped (see col. 5, lines 61-64). And, it is art-known that the terms of "n+" and "N+" both have the same meaning of being a degenerately or heavily doped N type region.

Regarding the third and fourth arguments, Litwin clearly teaches that the well region 22 in the cited embodiment of Fig. 2) is formed by design as a p-type region (see col. 4, lines 9-13) in an NMOS-enhancement-transistor-type varactor. And, such an NMOS-enhancement-transistor-type structure naturally has n+ source/drain regions (23 and 24) with a p-type channel region (the top portion of the well region 22) therebetween, regardless whether the threshold implantation of the CMOS is blocked, since such threshold implantation is normally in a separated process step from the process step of forming the P-type well. In fact, both Chiang (col. 5, lines 1-10) and Litwin (col. 5, lines 36-40) teach to keep the channel region as a lightly doped region. And, it would have been well within the ordinary skill in the art to incorporate the making of the P-type lightly doped well or body regions of Litwin into the method of Chinag, as

the resulting structure is an art-known NMOS-enhancement-transistor type, which makes a varactor with a commonly desired highly sensitive depletion-type channel regions. And, with the P-type lightly doped regions in the above collectively taught method, N+/P- junctions would be naturally formed therein.

Regarding applicant's arguments concerning claim 34, as noted in the previous office action that SOI type substrate, i.e., silicon-on-oxide type substrate is an art-known common substrate for achieving high performance for MOS type device structure, as evidenced in the prior art such as Tsang (US 5,563,438; see col. 3, lines 36-37) already provided in the previous office action. And, it is art-known that such a SOI type substrate normally naturally includes a highly resistive silicon bottom layer, as further evidenced in prior art reference of Hull et al. (US 6,172,378; see col. 4, lines 10-18; of record, see the 05-16-03 IDS).

Regarding applicant's arguments concerning claim 37, with the well being formed with P type in the collectively taught varactor above, the body therein would naturally be allowed to float due the existence of the PN junctions formed between the body region and the source/drain regions.

Regarding claims 39 and 40, as noted in the claim rejections above, the silicon gates in Litwin can have a width-to-length ratio in a range covering a ratio of approximately 16 to 1 (see col.6, lines 10-17), which is substantially the same ratio as that in the instant invention. It would naturally result in a capacitor switching ratio in the varactor collectively taught above substantially similar to that of the instant invention, insofar as the recited ratio being supported by the original disclosure. Besides, it is art-

known that high capacitor switching ratio is always commonly desirable; and it would be well within the ordinary skill in the art to make and optimize the varactor structure collectively taught above so as to achieve a capacitor switching ratio as high as or higher than the one recited in the instant invention.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
December 10, 2004

SHOUXIANG HU
PRIMARY EXAMINER